

Docket No.: M4065.0381/P381-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Leonard Forbes, et al.

Application No.: Not Yet Assigned

Group Art Unit: N/A

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: TECHNIQUE TO MITIGATE SHORT
 CHANNEL EFFECTS WITH VERTICAL
 GATE TRANSISTOR WITH DIFFERENT
 GATE MATERIALS

INFORMATION DISCLOSURE STATEMENT (IDS)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO/SB/08 are not supplied because they were previously cited by or submitted to the Office in a prior application no.09/808,114 filed March 15, 2001, and relied upon in this application for an earlier filing date under 35 U.S.C. § 120.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 C.F.R. § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

The Commissioner is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0381/P381. A duplicate copy of this paper is enclosed.

Dated: January ~~23~~
28, 2004

Respectfully submitted,

By 

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Approved for use through 10/31/2002.OMB 0651-0031

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Substitute for form 1449A/PTO <h1>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</h1> <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	
				First Named Inventor	Leonard Forbes
				Group Art Unit	2826
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	M4065.0381/P381-A
Sheet	1	of	2		

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		5,356,821		Naruse et al.	10/1994	
		5,886,368		Forbes et al.	03/1999	
		6,097,070		Mandelman et al.	08/2000	
		6,274,510		Wilk et al.	08/2001	
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		6,563,151		Shin et al.	05/2003	
		6,114,736		Balasubramanyam et al.	09/2000	
		6,281,559		Yu et al.	08/2001	

[illegible]

Examiner Signature		Date Considered	
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¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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		Filing Date			
		First Named Inventor	Leonard Forbes		
		Group Art Unit	N/A		
		Examiner Name	Not Yet Assigned		
Sheet	2	of	2	Attorney Docket Number	M4065.0381/P381

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A	S. Tiwari, et al., "Straddle Gate Transistors: High I_{on}/I_{off} Transistors at Short Gate Lengths" IBM Research Division.	
	B	W. Long, et al., "Dual-Material Gate (DMG) Field Effect Transistor."	
	C	N. R. Rueger, et al. "Selective Etching of SiO ₂ Over Polycrystalline Silicon Using CHF ₃ in an Inductively Coupled Plasma Reactor."	
	D	S. Vallon, et al., "Polysilicon-germanium Gate Patterning Studies in a High Density Plasma Helicon Source", J. Vac. Sci. Technol. A 15(4), Jul/Aug 1997.	
	E	P. Patel, et al., "Low Temperature VUV Enhanced Growth of Thin Silicon Dioxide Films" Applied Surface Science 46 (1990) 352-356.	
	F	W. Shindo, et al., "Low-Temperature Large-Grain Poly-Si Direct Deposition by Microwave Plasma Enhanced Chemical Vapor Deposition Using SiH ₄ /Xe", J. Vac. Sci. Technol. A 17(5), Sep/Oct 1999.	
	G	R. Nozawa, et al., "Low Temperature Polycrystalline Silicon Film Formation With and Without Charged Species in an Electron Cyclotron Resonance SiH ₄ /H ₂ Plasma-Enhanced Chemical Vapor Deposition", J. Vac. Sci. Technol. A 17(5), Sep/Oct 1999.	
	H	C. Saha, et al., "Ion Assisted Growth and Characterization of Polycrystalline Silicon and Silicon-Germanium Films" (visited Nov. 18, 1999) < http://www.dialogselect.com/tech/cgi/pres >.	
	I	D. Landheer, et al., "Formation of High-Quality Silicon Dioxide Films by Electron Cyclotron Resonance Plasma Oxidation and Plasma-Enhanced Chemical Vapour Deposition" (visited Oct. 21, 1999) < http://www.dialogselect.com/tech/cgi/pres >.	
	J	K. Usami, et al., "Thin Si Oxide Films for MIS Tunnel Emitter by Hollow Cathode Enhanced Plasma Oxidation" (visited Oct. 21, 1999) < http://www.dialogselect.com/tech/cgi/pres >.	
	K	K.C. Saraswat, et al. "A Low Temperature Polycrystalline SiGe CMOS TFT Technology for Large Area AMLCD Drivers" (visited 11/18/99) < http://www.dialogselect.com/tech/cgi/pres >.	

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